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| 10/537,211 | 03/20/2006 | Uwe Schwarz | D4695-00135 | 1865 |

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| EXAMINER | |
|---|---|
| PATEL, REEMA | |
| **ART UNIT** | **PAPER NUMBER** |
| 2812 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/537,211 | SCHWARZ, UWE | |
| | Examiner | Art Unit | |
| | Reema Patel | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) was submitted on 3/20/06. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5-6, and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Parameswaran et al. ("A Merged MEMS-CMOS Process using Silicon Wafer Bonding").

5. Regarding claim 1, Parameswaran et al. discloses the following claimed elements:

- A method for forming microelectromechanical sensors (MEMS), wherein the sensors and the sensor signal processing electronics are monolithically integrated, comprising:

- (i) firmly connecting a first silicon wafer having cavities formed thereon with a second cap wafer having an epitaxial layer by means of high temperature fusion bonding via the epitaxial layer (page 23.6.1, col 2, lines 32-41),
- (ii) wherein the wafer composite is reduced from the second wafer towards the epitaxial layer, that is, to a membrane thickness corresponding to the micromechanical portion of the sensor or to a thickness of another portion of the semiconductor wafer responding to mechanical stress, and wherein the wafer composite is finally polished (page 23.6.1, col 2, lines 41-45),
- (iii) wherein after the polishing process, the electronic sensor structures registered to the cavity are commonly formed along with the analogous or/and digital circuitries on the polished surface by means of CMOS technology methods (page 23.6.1, col 2, lines 45-46 – page 23.5.2, col 1, lines 1-4).

6. Regarding claim 5, Parameswaran et al. discloses the following claimed elements:

- A method for forming a microelectromecanical sensor or system (MEMS), wherein at least one sensor and an associated sensor processing electronic are monolithically integrally formed,
  - (i) by bonding a first wafer comprising at least one cavity with a second wafer carrying an epitaxial layer by means of a high temperature fusion

bonding process via the epitaxial layer to form a composite of the wafers (page 23.6.1, col 2, lines 32-41);

- (ii) wherein the composite of the wafers is thinned from the second wafer down to the epitaxial layer and is finally polished (page 23.6.1, col 2, lines 41-45);
- (iii) wherein after the polishing process at least one sensor structure aligned to the cavity and at least one analogous or/and digital circuit on the polished surface are formed by means of a CMOS technology method (page 23.6.1, col 2, lines 45-46 – page 23.5.2, col 1, lines 1-4).

7. Regarding claim 6, Parameswaran et al. discloses that the thinning is performed according to a membrane thickness corresponding to the micromechanical portion of the sensor according to a thickness of another portion of the semiconductor wafer that is sensitive or responsive to a mechanical stress (page 23.6.1, col 2, lines 36-39).

8. Regarding claim 10, Parameswaran et al. discloses the following claimed elements:

- A micromechanical sensor or system (MEMS), wherein at least one sensor and associated sensor signal processing electronics are monolithically integrally formed,
  - (i) by bonding the first wafer comprising at least one cavity to a second wafer carrying an epitaxial layer by means of a high temperature fusion bonding process via the epitaxial layer so as to form a composite of the wafers (page 23.6.1, col 2, lines 32-41);

- (ii) by reducing the composite of the wafers from the second wafer down to the epitaxial layer and by polishing the same (page 23.6.1, col 2, lines 41-45);
- (iii) wherein a mechanical sensor structure is aligned to the cavity and is commonly provided with an analogous or/and digital circuit on the polished surface at least partially in the thinned epitaxial layer, formed prior to or after the polishing process by means of a monolithic integrating technology method (page 23.6.1, col 2, lines 45-46 – page 23.5.2, col 1, lines 1-4).

9. Regarding claim 11, Parameswaran et al. discloses that the thinning is performed to obtain the thickness of a membrane (page 23.6.1, col 2, lines 41-45).

10. Regarding claim 12, Parameswaran et al. discloses that the circuit structure is provided prior to or during bonding (page 23.6.1, col 1 lines 5-7).

11. Regarding claim 13, Parameswaran et al. discloses that the technology method is a CMOS technique (page 23.6.1, col 2, lines 45-46 – page 23.5.2, col 1, lines 1-4).

## *Claim Rejections - 35 USC § 103*

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 2-4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parameswaran et al. ("A Merged MEMS-CMOS Process using Silicon Wafer Bonding") as applied to claims 1 and 5 above, respectively, and further in view of Black et al. (U.S. 4,463,336).

14. Regarding claims 2 and 7, Parameswaran et al. discloses the limitations of claim 1 and 5, and that there are electronic circuits but does not disclose such circuits are on that side of the epitaxial layer that faces the cavity after the bonding process (Fig. 2). However, Black et al. discloses forming electronic circuitry structures on the side of the epitaxial layer that faces the cavity after the bonding process (Fig. 8-9; col 5, lines 25-55) for the advantage of creating a reliable, electronic pressure sensor which can be mass produced at low cost (col 1, lines 41-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Parameswaran et al. with forming the electronic circuitry structures on the side of the epitaxial layer that faces the cavity, as taught by Black et al., so as to create a reliable and low cost electronic pressure sensor.

15. Regarding claims 3 and 8, Black et al. discloses that the electronic structures formed on the side facing the cavity after the wafer bonding process extend to the polished side to form electrically conductive channels (Fig. 8; col 5, lines 25-55).

16. Regarding claims 4 and 9, Black et al. discloses that the electronic structures created at the side facing the cavity comprise specific sensors in particular for the analysis of the medium located adjacent to the membrane in the cavity (col 6, lines 34-40).

***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tilmans et al. (U.S. 6,297,072 B1) discloses a method of fabricating a microstructure having an internal cavity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reema Patel whose telephone number is 571-270-1436. The examiner can normally be reached on M-F, 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RSP
5/11/07

SCOTT B. GEYER
PRIMARY EXAMINER

5/14/07